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MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
DARE, RYAN A	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/613,542	PARK ET AL.	
	Examiner	Art Unit	
	RYAN DARE	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,30,46 and 47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,30,46 and 47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-28, 30, and 46-47 are rejected under 35 U.S.C. 102(e) as being anticipated by Pereira et al., US Patent 6,542,391.

3. With respect to claim 1, Pereira teaches a content addressable memory (CAM) device, comprising: a priority resolution circuit that is configured to hierarchically resolve competing soft priorities between a plurality of active hit signals according to numeric significance so that a first of the plurality of active hit signals having a first priority will block resolution of a second of the plurality of active hit signals having a second priority when the first priority is higher than the second priority and vice versa when the second priority is higher than the first priority, in col. 19, lines 27-53, and col. 21, lines 9-29.

4. With respect to claim 2, Pereira teaches the CAM device of Claim 1, wherein said priority resolution circuit is configured to resolve competing hard priorities between two or more of the plurality of active hit signals having equivalent highest soft priorities by

identifying which of the two or more of the plurality of active hits signals has the highest hard priority, in col. 35, lines 13-28, the row priority circuit.

5. With respect to claim 3, Pereira teaches the CAM device of Claim 2, wherein said priority resolution circuit comprises a MSB soft priority resolution stage and a LSB soft priority resolution stage, in col. 20, lines 5-20.

6. With respect to claim 4, Pereira teaches the CAM device of Claim 3, wherein said priority resolution circuit comprises a hard priority resolution stage electrically coupled to outputs of said LSB soft priority resolution stage; and wherein said priority resolution circuit is further configured so that competing and unequal soft priorities of at least some of the plurality of active hit signals are completely resolved by the MSB and LSB soft priority resolution stages prior to further resolution of hard priority by the hard priority resolution stage, in col. 20, lines 5-20.

7. With respect to claim 5, Pereira teaches the CAM device of Claim 1, further comprising: a plurality of CAM array blocks having respective soft priorities assigned thereto; wherein said priority resolution circuit comprises a plurality of registers that retain the soft priorities assigned to said plurality of CAM array blocks; and wherein said priority resolution circuit is configured so that the soft priorities retained by the plurality of registers can be arranged in any order regardless of the values of hard priorities assigned to said plurality of CAM array blocks, in col. 19, lines 27-53.

8. With respect to claim 6, Pereira teaches a content addressable memory (CAM) device, comprising: a plurality of CAM array blocks having respective soft priorities assigned thereto; and a hierarchical priority resolution circuit that is configured to

identify a highest priority one of said plurality of CAM array blocks having respective matching entries therein during a search operation, by sequentially evaluating the soft priorities of said plurality of CAM array blocks according to numeric significance so that matching entries in a first of said plurality of CAM array blocks are treated as having higher priority than matching entries in a second of said plurality of CAM array blocks when the soft priority of the first of said plurality of CAM array blocks is hiqher than the soft priority of the second of said plurality of CAM array blocks and vice versa when the soft priority of the second of said plurality of CAM array blocks is higher than the soft priority of the first of said plurality of CAM array blocks, in col. 19, lines 27-53.

9. With respect to claim 7, Pereira teaches the CAM device of Claim 6, wherein said hierarchical priority resolution circuit is configured to sequentially evaluate the soft priorities of said plurality of CAM array blocks in descending order according to numeric significance, in col. 19, lines 27-53 and col. 20, lines 5-20.

10. With respect to claim 8, Pereira teaches the CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises a plurality of programmable registers that retain the soft priorities; and wherein said hierarchical priority resolution circuit is configured so that the soft priorities retained by the plurality of programmable registers can be arranged in any order regardless of the values of hard priorities assigned to said plurality of CAM array blocks, in col. 19, lines 27-53.

11. With respect to claim 9, Pereira teaches the CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises: a first soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines; and a

second soft priority resolution circuit that is electrically coupled in a wired-OR manner to a second plurality of signal lines, in col. 29, lines 23-28.

12. With respect to claim 10, Pereira teaches the CAM device of Claim 9, wherein the first and second plurality of signal lines are floated or biased at precharged levels during the search operation, in col. 9, lines 17-18.

13. With respect to claim 11, Pereira teaches the CAM device of Claim 9, wherein said hierarchical priority resolution circuit further comprises: a third soft priority resolution circuit that is electrically coupled in a wired-OR manner to a third plurality of signal lines, in col. 9, lines 17-18.

14. With respect to claim 12, Pereira teaches the CAM device of Claim 11, wherein said hierarchical priority resolution circuit further comprises: a hard priority resolution circuit that is electrically coupled to outputs of said third soft priority resolution circuit, in col. 9, lines 4-27.

15. With respect to claim 13, Pereira teaches the CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises: a soft priority resolution circuit; and a hard priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit, in col. 19, lines 27-53.

16. With respect to claim 14, Pereira teaches the CAM device of Claim 6, wherein said hierarchical priority resolution circuit comprises: a soft priority resolution circuit that is electrically coupled in a wired-OR manner to a first plurality of signal lines that are floated or biased at precharged levels during a priority resolution operation; and a hard

priority resolution circuit that is electrically coupled to outputs of said soft priority resolution circuit, in col. 19, lines 27-53 and col. 9, lines 4-27.

17. With respect to claim 15, Pereira teaches a content addressable memory (CAM) device, comprising: a priority resolution circuit configured to resolve competing soft priorities between a plurality of active hit signals associated with a respective plurality of CAM array blocks, in response to a search operation , said priority resolution circuit further configured to support all orders of priority between the plurality of CAM array blocks so that a first of the plurality of active hit signals having a first soft priority will block resolution of a second of the plurality of active hit signals having a second priority when the first priority is higher than the second priority and vice versa when the second priority is higher than the first priority, in col. 19, lines 27-53.

18. Claims 16-18 are similar to claims 2-4 and are rejected using similar logic.

19. Claim 19 is similar to claims 1 and 2, and is rejected using similar logic.

20. With respect to claim 20, Pereira teaches the CAM device of Claim 19, wherein the competing soft priorities of the plurality of active hit signals are resolved by evaluating the soft priorities in a MSB to LSB sequence, in col. 9, lines 36-42.

21. With respect to claim 21, Pereira teaches the CAM device of Claim 19, wherein said priority resolution circuit is a hierarchical priority resolution circuit having at least two soft priority resolution stages and a hard priority resolution stage, in col. 6, lines 22-67.

22. Claim 22 is similar to claim 6 and is rejected using similar logic.

23. Claim 23 is similar to claims 1 and 2 and is rejected using similar logic.

24. With respect to claim 24, Pereira teaches a content addressable memory (CAM) device, comprising: a plurality of CAM array blocks that each have respective soft and hard priorities assigned thereto; and a priority resolution circuit configured to resolve competing soft priorities for all possible combinations of soft priority order between said plurality of CAM array blocks and further configured to resolve competing hard priorities between at least two of said plurality of CAM array blocks having the same soft priority, during an operation to search the plurality of CAM array blocks to identify respective matching entries therein, in col. 20, lines 5-20 and col. 21, lines 9-29.

25. With respect to claim 25, Pereira teaches the CAM device of Claim 24, wherein the CAM device comprises 2N+1 CAM array blocks therein, where N is an integer; and wherein said priority resolution circuit comprises log2N groups of precharged signal lines that are used during a priority resolution operation to resolve competing soft priorities between hit signals generated by said plurality of CAM array blocks, in col. 19, lines 27-53 and col. 25, lines 22-25.

26. With respect to claim 26, Pereira teaches the CAM device of Claim 24, wherein the CAM device comprises 2N+1 CAM array blocks, where N is an integer; and wherein said priority resolution circuit comprises log2N groups of N or N-1 precharged signal lines, in col. 25, lines 22-25.

27. With respect to claim 27, Pereira teaches the CAM device of Claim 24, wherein the CAM device comprises (2x)y CAM array blocks, where x and y are integers; and wherein said priority resolution circuit comprises y groups of precharged signal lines having 2x or 2x-1 signal lines per group, in col. 5, lines 22-25

28. With respect to claim 28, Pereira teaches the CAM device of Claim 27, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2), in col. 5, lines 22-25.

29. With respect to claim 30, Pereira teaches a content addressable memory (CAM) device, comprising: a plurality of CAM array blocks that each have having respective soft priorities associated therewith that are programmable and respective hard priorities associated therewith that are fixed according to layout position; and a soft priority resolution circuit configured to process first and second active hit signals generated by first and second CAM array blocks within said plurality of CAM array blocks during a search operation, respectively, using wired- OR logic to identify a highest priority one of the first and second active hit signals and selectively block another one of the first and second active hit signals from being further processed as a highest priority candidate; wherein said wired-OR logic is configured to support all possible combinations of soft priority order between said plurality of CAM array blocks, in col. 19, lines 27-53, and col. 21, lines 9-29.

30. With respect to claim 46, Pereira teaches a content addressable memory (CAM) device, comprising: (2×)y CAM array blocks; and a soft priority resolution circuit that hierarchically resolves competing soft priorities between a plurality of active hit signals generated _bY a plurality of the CAM array blocks during a search operation and comprises y groups of precharged signal lines having 2x or 2x-1 signal lines per group that support soft priority resolution of all possible combinations of soft priority order between the plurality of active hit signals, in col. 19, lines 27-53, and col. 21, lines 9-29.

31. With respect to claim 47, Pereira teaches the CAM device of Claim 46, wherein x and y represent a pair of integers selected from the pair groups (x,y) consisting of (3,3), (2,4) and (3,2), in col. 19, lines 27-53, and col. 21, lines 9-29.

Response to Arguments

32. Applicant's arguments filed 2/11/09 have been fully considered but they are not persuasive. Applicant describes the advantages of his own invention, mainly that there are N-factorial combinations of priority order possible. This limitation is not recited in the independent claims, and it would be improper to read this limitation into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant does not point to any particular limitation of the claims that Pereira et al. does not teach so Applicant's arguments amount to a mere allegation of patentability. The examiner believes that Pereira does in fact teach the limitations of the amended claims, looking particularly at col. 19, lines 27-53, and col. 21, lines 9-29. This section shows that the normal chain priority is used, but in one case, the CAM Block 802(0) could be given the priority of 11. Therefore Pereira does teach all limitations of the amended claims.

Conclusion

33. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar memory systems.

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RYAN DARE whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

/Ryan Dare/
May 21, 2009